Remarks

In the Office action, claims 1, 2, 5-8, and 11-12 were rejected as anticipated by Lin (US 6,740,557). Claims 3-4 and 9-10 were rejected as unpatentable over Lin in view of Burns et al. (US 6,258,679). In the forgoing, claim 1 has been amended to recite that forming the sacrificial layer occurs after forming a gate oxide. New claim 13 has been added to include the limitation that the sidewall gates are divided by a trench. In view of the forgoing amendments and the following remarks, reconsideration of the application is respectfully requested.

Claim 1 recites, *inter alia*, a method of forming a gate in a semiconductor device, wherein the method includes forming on a semiconductor substrate a gate oxide layer and then forming on a semiconductor substrate a sacrificial layer.

Lin is directed to a spacer-like floating gate formation. Lin discloses that, "[a] dielectric layer (110), is ... formed over the substrate." (Col. 4, lines 63-63). "[An] opening for the floating area is formed by etching the structural layer, thus transferring opening (125) in the photomask into layer (110) to form opening (115)." (Col. 4, lines 13-16) "Tunnel oxide (130) is next grown at the bottom of opening (115) by thermal growth." (Col. 5, lines 19-20) Lin does not, however, disclose or suggest forming on a semiconductor substrate a gate oxide layer and then forming on a semiconductor substrate a sacrificial layer. Even if the tunnel oxide 130 of Lin is considered to be a gate oxide layer and the dielectric layer 110 of Lin is considered to be a sacrificial layer, which is not conceded by the applicants, Lin still does not disclose or suggest that the dielectric layer 110 is formed after the tunnel oxide 130 is formed. To the contrary, Lin teaches that the tunnel oxide 130 is formed in an opening 115

created in the dielectric layer 110. Therefore, the tunnel oxide 130 cannot possibly be formed until after the dielectric layer 110 is formed.

The Office action also cites Burns, but Burns cannot cure the deficiency of Lin described above. Similar to Lin, Burns teaches that a nitride layer 16 is formed, the nitride layer 16 is etched to form a hole, and the gate oxide layer 22 is formed in the hole. "As shown in FIG. 1F, element 22 is a thin oxide layer (thickness of 3nm or less) which represents the gate oxide of the FET." (Col. 4, lines 65-67) Because the gate oxide layer is formed in the hole etched in the nitride layer, the nitride layer cannot be formed after the gate oxide layer, as recited in claim 1. Thus, both Lin and Burns are missing the same element. Therefore, no combination of these references can result in the claimed process and the claims are patentable over Lin in view of Burns.

Additionally, claim 13 recites that the sidewall gate electrodes are divided by a trench as shown in FIGS. 1a-1d. Lin discloses that two floating gates are formed on a common source and are formed in the same active region. Lin does not disclose that sidewall gate electrodes are separated by a STI. Rather, Lin discloses that floating gates may be separated by a source 103 or a drain 107. Therefore, claim 13 is not anticipated by Lin. Additionally, Burns does not disclose or suggest that the two gates are separated by a shallow trench isolation. Thus, Burns cannot anticipate claim 13.

For at least the forgoing reason, independent claim 1 and claims 2-13 dependent thereon are patentable over the cited art. Accordingly, reconsideration of the application and allowance thereof is respectfully requested. If there is any matter that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,

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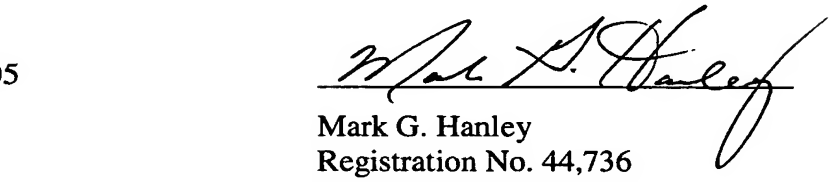

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